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10/803,162	03/18/2004	David Raymond Lutz	550-536	4162

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/803,162	LUTZ ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 01/01/2007.

2. Claims 1-22 are pending in this application. Claims 1 and 12 are independent claims. This Office Action is made non-final.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title:

4. Claims 1-22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-22 cite a method and apparatus for computing absolute difference of numbers in accordance with a mathematical algorithm. In order for claims to be statutory, claims must either include a practical/physical application or a concrete, useful, and tangible result. However, claims 1-22 merely disclose steps/components for computing absolute difference of numbers without further disclosing a practical/physical application or a useful and tangible result since the claims appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein. In addition,

the logic in claims 1-11 can be software logic. Therefore, claims 1-22 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (U.S. 6,578,060).

Re claim 1, Chen et al. disclose in Figures 1-19 a data processing apparatus (e.g. abstract and Figure 1, particularly part 15 of Figure 1) comprising: processing logic (e.g. components 1-3 in Figure 1) operable to perform a data processing operation on first and second data elements (e.g. EA and EB), the processing logic comprising: comparison logic (e.g. component 202 in Figure 7) operable to compare at least a part of the first and second data elements (e.g. EA and EB respectively) in order to determine which of the first and second data elements is a larger data element (e.g. CA>CB?), the comparison logic being operable to produce a comparison result which has a first value if the first data element is the larger data element and a second value if the second data element is the larger data element (e.g. output of component 202 in Figure 7 wherein the output will be 0 if EA>EB otherwise the output will be 1); absolute difference logic operable to compute an absolute difference between a portion of the first data element and a portion

of the second data element (e.g. components 201, 103, and 104 in Figure 7), the absolute difference logic comprising: adder logic operable to invert one of said portions to produce an inverted data element portion (e.g. Figures 4 and 8 wherein it inverts the second operand as /IB) and to add the inverted data element portion to the other of said portions (e.g. IA as other portion) and to the comparison result (e.g. either 0/1 corresponding to the comparison of component 202 in Figure 7) received from the comparison logic in order to produce an intermediate result (e.g. output of component 201 in Figure 7); and output logic operable to generate an inverted version of the intermediate result (e.g. by inverter 103 in Figure 7) and to output as the absolute difference either the intermediate result or the inverted version of the intermediate result dependent on the comparison result (e.g. output of 104 as the mux to yield |EA-EB| in Figure 7).

Re claim 2, Chen et al. further disclose in Figures 1-19 the adder logic is operable to invert the portion of the second data element (e.g. by component 103 in Figure 7), and the comparison result is set to a logic 0 value if the second data element is the larger data element, and is set to a logic 1 value otherwise, the output logic being operable to output as the absolute difference the inverted version of the intermediate result if the comparison result has a logic 0 value (e.g. output of component 202 in Figure 7 wherein the output will be 0 if EA>EB otherwise the output will be 1), and to output as the absolute difference the intermediate result if the comparison result has a logic 1 value (e.g. either 0/1 corresponding to the comparison of component 202 in Figure 7).

Re claim 3, Chen et al. further disclose in Figures 1-19 the comparison result is set to the first value if the first data element and the second data element have the same value (e.g. CA>CB? only as seen in Figure 7).

Re claim 4, Chen et al. further disclose in Figures 1-19 the comparison logic is operable to perform a non-redundant subtract operation on said at least a part of the first and second data elements, and the comparison result comprises a carry out result of the non-redundant subtract operation (e.g. Figure 7).

Re claim 5, Chen et al. further disclose in Figures 1-19 the first and second data elements are floating point data elements, the first floating point data element specifying a first significand and the second floating point data element specifying a second significand, and the absolute difference logic being operable to compute the absolute difference between the first significand and the second significand (e.g. abstract and Figure 1).

Re claim 6, Chen et al. further disclose in Figures 1-19 each of the first and second floating point data elements comprise sign, exponent and fraction portions (e.g. SA, EA, and FA of component 2 in Figure 1), the first and second significands being derived from the corresponding fraction portions of the first and second floating point data elements, the at least a part of the first and second data elements compared by the comparison logic comprising the exponent and fraction portions of the first and second floating point data elements (e.g. component 15 in Figure 1).

Re claim 7, Chen et al. further disclose in Figures 1-19 the data processing apparatus is operable to receive first and second operands (e.g. NA and NB in Figure 1 as

operands), the first operand comprising a plurality of said first floating point data elements (e.g. SA, EA, and FA in Figure 1), and the second operand comprising a corresponding plurality of said second floating point data elements (e.g. SB, EB, and FB in Figure 1), said comparison logic and said absolute difference logic being replicated within the data processing apparatus for each pair of first and second floating point data elements provided by the first and second operands (e.g. component 4 in Figure 1 and its corresponding Figure 7).

Re claim 8, Chen et al. further disclose in Figures 1-19 the first and second data elements are integer data elements (e.g. purely Figure 7 wherein EA and EB are just integers), and the portion of the first and second data elements that the absolute difference logic is operable to compute the absolute difference for is the entirety of the first and second integer data elements (e.g. components 202 and 201 in Figure 7).

Re claim 9, Chen et al. further disclose in Figures 1-19 the at least a part of the first and second data elements compared by the comparison logic comprises the entirety of the first and second integer data elements (e.g. Figure 7).

Re claim 10, Chen et al. further disclose in Figures 1-19 the data processing apparatus is operable to receive first and second operands (e.g. EA and EB as operands), the first operand comprising a plurality of said first integer data elements (e.g. EA), and the second operand comprising a corresponding plurality of said second integer data elements (e.g. EB), said comparison logic being operable to receive the first and second operands and to produce, for each pair of first and second integer data elements provided by the first and second operands, an associated comparison result (e.g. Figure 7).

Re claim 11, Chen et al. further disclose in Figures 1-19 the absolute difference logic is operable to receive the first and second operands (e.g. EA and EB respectively); the adder logic is operable to invert one of the first and second operands to produce a plurality of inverted integer data elements (e.g. Figures 4 and 8 wherein EB as IB is inverted as /IB) and, for each pair of first and second integer data elements, to add the associated inverted data element to the other of the first and second data elements (e.g. IA as EA + /IB as /EB) and to the associated comparison result (e.g. as corresponding to Cin 0/1) received from the comparison logic in order to produce an associated intermediate result (e.g. output of component 201 in Figure 7); and the output logic is operable to generate an inverted version of each associated intermediate result (e.g. by inverter 103 in Figure 7) and, for each pair of first and second integer data elements, to output as the associated absolute difference either the associated intermediate result or the inverted version of the associated intermediate result dependent on the associated comparison result (e.g. by the mux 104 for selecting the correct absolute difference result).

Re claim 12, it is a method claim of claim 1. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 13, it is a method claim of claim 2. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 14, it is a method claim of claim 3. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 15, it is a method claim of claim 4. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 16, it is a method claim of claim 5. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 17, it is a method claim of claim 6. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 18, it is a method claim of claim 7. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 19, it is a method claim of claim 8. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 20, it is a method claim of claim 9. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 21, it is a method claim of claim 10. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 22, it is a method claim of claim 11. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Response to Arguments

7. Applicant's arguments filed 08/01/2007 have been fully considered but they are not persuasive.

a. The applicant extensively argues in page 14 for claims rejected under 35 U.S.C. 102(b) that the cited reference by Chen et al. fails to disclose the structure of independent claims, particularly the adder for adding the inverted data element portion to the other of

said portions and to the comparison result received from the comparison logic, as cited in the claimed invention.

The examiner respectfully submits that the third term, the comparison result received from the comparison logic, is internally imbedded into the difference of numbers as seen in Figures 6 and 9 as adding logic 1/0 depending on algorithm as seen in Figures 4 and 8.

b. The applicant argues in page 15 for claims rejected under 35 U.S.C. 102(b) that the cited reference by Chen et al. further fails to disclose or define the output logic operable to generate an inverted version of the intermediate result...since the result of the cited reference is approximated result and it would correct later using the compensating shift circuit as seen in Figure.

The examiner respectfully submits that Figures 2 and 7, as alleged by the applicant, would yield correct absolute difference of numbers with the following reasons. First, last limitation of independent claims requires only to output the absolute difference either <<as alternate form>> the intermediate result or the inverted version of the intermediate result wherein the claims do not clearly define or requires the intermediate result is an exact solution of the absolute difference or an approximate solution of the absolute difference. Further, the claims require only either one of the two output forms. Thus, either Figures 2 or 7 of the cited reference by Chen et al. clearly disclose the last limitation cited by the claimed invention. In Figure 2, the output of multiplexer 104 can the output

terminal input 1 as the exact result of absolute difference of numbers (EA-EB) or the output terminal input 0 as the approximate (e.g. by symbol only) of absolute difference of numbers wherein the output of inverter 103 must be output of inverted absolute difference of numbers (EA-EB) since it takes the same input as (EA-EB) directly. In Figure 7 with same analogous reasoning as above, the output of multiplexer 104 clearly and absolutely will output the difference of number accordingly. The compensating shift circuit does not involve in the process of computing absolute difference of numbers as alleged by the applicant because the output of shifting circuit does not input into the absolute difference of number circuit at all as clearly seen in Figures 2 or 7.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

October 14, 2007